NANO SCIENTIFIC RESEARCH CENTRE

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VLSI: M.Tech/M.E IEEE Project List – 2017-18

CODE	M.Tech VLSI IEEE PROJECTS	YEAR
NV1701	Probability-Driven Multibit Flip-Flop Integration with Clock Gating.	2017
NV1702	Area-Time Efficient Architecture of FFT Based Montgomery Multiplication	2017
NV1703	Reliable Low-Latency Viterbi Algorithm Architectures Benchmarked on ASIC and FPGA	2017
NV1704	Improved 64-bit Radix-16 Booth Multiplier Based on Partial Product Array Height Reduction	2017
NV1705	Weighted Partitioning for Fast Multiplier less Multiple-Constant Convolution Circuit	2017
NV1706	Probabilistic Error Modeling for Approximate Adders	2017
NV1707	LFSR-Based Generation of Multicycle Tests	2017
NV1708	Clock-Gating of Streaming Applications for Energy Efficient Implementations on FPGAs	2017
NV1709	RoBA Multiplier: A Rounding-Based Approximate Multiplier for High-Speed yet Energy-Efficient Digital Signal Processing	2017
NV1710	High-Throughput and Energy-Efficient Belief Propagation Polar Code Decoder	2017
NV1711	Design of Power and Area Efficient Approximate Multipliers	2017
NV1712	High-Speed Parallel LFSR Architectures Based on Improved State-Space Transformations	2017
NV1713	Scalable Approach for Power Droop Reduction During Scan-Based Logic BIST	2017
NV1714	Sign-Magnitude Encoding for Efficient VLSI Realization of Decimal Multiplication	2017
NV1715	Reconfigurable Constant Multiplication for FPGAs	2017
NV1716	Digit-Level Serial-In Parallel-Out Multiplier Using Redundant Representation for a Class of Finite Fields	2017

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CODE	M.Tech VLSI IEEE PROJECTS	YEAR
NV1601	Floating-Point Butterfly Architecture Based on Binary Signed-Digit Representation	2016
NV1602	Flexible DSP Accelerator Architecture Exploiting Carry-Save Arithmetic	2016
NV1603	Utilizing Shared Memory Multi-cores to Speed-up the ATPG process	2016
NV1604	Fault Tolerant Parallel Filters Based on Error Correction Codes	2016
NV1605	Error Correction Technique Based on Modular Correcting Codes	2016
NV1606	FPGA Based Rate Compatible LDPC Codes for The Next Generation of Optical Transmission Systems	2016
NV1607	A Modified Partial Product Generator for Redundant Binary Multipliers	2016
NV1608	A High-Throughput Energy-Efficient Implementation of Successive Cancellation Decoder for Polar	2016
NV1609	On Optimization-based ATPG and its Application for Highly Compacted Test Sets	2016
NV1610	High-Performance Pipelined Architecture of Elliptic Curve Scalar Multiplication Over GF(2^m)	2016
NV1611	Fault Tolerant Parallel FFTs Using Error Correction Codes and Parseval Checks	2016
NV1612	A High-Throughput Energy-Efficient Implementation of Successive Cancellation Decoder for Polar	2016
NV1613	Low-Power Parallel Chien Search Architecture Using a Two-Step Approach	2016
NV1614	Memory-Reduced Turbo Decoding Architecture Using NII Metric Compression Logic	2016
NV1615	A Normal I/O Order Radix-2 FFT Architecture to Process Twin Data Streams for MIMO	2016
NV1616	A High-Performance FIR Filter Architecture for Fixed and Reconfigurable Applications	2016

VLSI: M.Tech/M.E IEEE Project List – 2015

CODE	M.Tech VLSI IEEE PROJECTS	YEAR
NV1501	ADynamicallyReconfigurableMulti-ASIPArchitectureforMultistandard and Multimode Turbo Decoding	2015
NV1502	Low-Cost High-PerformanceVLSIArchitectureforMontgomeryModular Multiplication	2015
NV1503	Functional Constraint Extraction From RegisterTransferLevel for ATPG	2015

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NV1504	Fault Tolerant Parallel Filters Based on Error Correction Codes	2015
NV1505	DScanPUF: A Delay-Based Physical Unclonable Function Built Into Scan Chain	2015
NV1506	Pre-Encoded Multipliers Based on Non-Redundant Radix-4 Signed-Digit Encoding	2015
NV1507	Quantumcostrealizationofnewreversiblegateswithtransformationbased synthesis technique	2015
NV1508	On the Analysis of Reversible Booth's Multiplier	2015
NV1509	Optimized Logarithmic Barrel Shifter in Reversible Logic Synthesis	2015
NV1510	A novel delay& Quantum Cost efficientreversiblerealizationof2i× j Random Access Memory	2015
NV1511	Exploiting Same Tag Bits to Improve the Reliability of the Cache Memories	2015
NV1512	Hardware Efficient MixedRadix-25/16/9FFT for LTE Systems	2015
NV1513	Energy-Efficient Approximate Multiplication for Digital Signal Processing and Classification Applications	2015(T)
NV1514	A Combined SDC-SDF Architecture for Normal I/O Pipelined Radix-2 FFT	2015(T)
NV1515	An Accuracy-Adjustment Fixed-Width Booth Multiplier Based on Multilevel Conditional Probability	2015(T)
NV1516	Design and ASIC Implementation of Column Compression Wallace/Dadda Multiplier in Sub-Threshold Regime	2015
NV1517	Novel Design Algorithm for Low Complexity Programmable FIR Filters Based on Extended Double Base Number System	2015(T)
NV1518	An Efficient VLSI Architecture of a Reconfigurable Pulse-Shaping FIR Interpolation Filter for Multistandard DUC	2015(T)
NV1519	(4 + 2 log n)ΔG Parallel Prefix Modulo-(2n − 3)Adder via Double Representation of Residues in [0, 2]	2015(T)
NV1520	Low-Complexity Tree Architecture for Finding the First Two Minima	2015(T)
NV1521	A Generalized Algorithm and Reconfigurable Architecture for Efficient and Scalable Orthogonal Approximation of DCT	2015(T)
NV1522	High-Throughput Finite Field Multipliers Using Redundant Basis for FPGA and ASIC Implementations	2015(T)
NV1523	Test Data Compression using Hamming Encoder and Decoder for System On Chip (SOC) Testing	2015

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NV1524	Self-Repairing Digital System With Unified Recovery Process Inspired by Endocrine Cellular Communication	2015(T)
NV1525	Fully Reused VLSI Architecture of FM0/Manchester Encoding Using SOLS Technique for DSRC Applications	2015(T)
NV1526	Partially Parallel Encoder Architecture for Long Polar Codes	2015(T)
NV1527	Z-TCAM: An SRAM-based Architecture for TCAM	2015(T)
NV1528	Digital Post-Correction of Analog-to-Digital Converters with Real-Time FPGA Implementation	2015(T)
NV1429	Low-Complexity Low-Latency Architecture for Matching of Data Encoded With Hard Systematic Error-Correcting Codes	2014(T)
NV1430	Energy-Efficient High-Throughput Montgomery Modular Multipliers for RSA Cryptosystems	2014(T)
NV1431	A Class of SEC-DED-DAE C Codes Derived From Orthogonal Latin Square Codes	2014
NV1432	Efficient FPGA and ASIC Realizations of a DA-Based Reconfigurable FIR Digital filter	2014
NV1433	Low-Power Digital Signal Processor architecture For WirelessSensorNodes	2014
NV1334	Error Detection in Majority Logic Decoding of Euclidean GeometryLow Density Parity Check(EG-LDPC)Codes	2013(T)
NV1335	Low-Power, High-Throughput, and Low-Area Adaptive FIR Filter Based On Distributed Arithmetic	2013(T)
NV1336	Radix-4andradix-8booth encoded multi-modulus multipliers	2013(T)
NV1337	Design and Implementation of an On-Chip Permutation Network for Multiprocessor System-On-Chip	2013(T)
NV1338	Multi operand Redundant Adders on FPGA's	2013
NV1339	Globalbuilt-inself-repairfor3Dmemorieswithredundancysharing and Parallel testing	2013
NV1340	A Practical NoC Design for Parallel DES Computation	2013
NV1341	Parallel AES Encryption Engines for Many-Core Processor Arrays	2013
NV1342	VLSI Implementation of a HighSpeedSinglePrecisionFloatingPointUnit Using Verilog	2013

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NV1343	A VLIW Architecture for Executing Multi-Scalar/Vector Instructions on Unified Data path	2013
NV1344	A Novel Modulo Adder for 2n-2k-1Residue Number System	2013(T)
NV1345	Low-cost FIR filter designs based on faithfully rounded truncated Multiple constant multiplication/accumulation	2013(T)
NV1346	Low-Power, High-Throughput, and Low-Area Adaptive FIR Filter Based On Distributed Arithmetic	2013(T)
NV1347	Design and Implementation of 32 Bit Unsigned Multiplier Using CLAA and CSLA	2013
NV1348	Enhanced Area Efficient Architecture for128 bit Modified CSLA	2013
NV1349	High Performance Hardware Implementation of AES Using Minimal Resources	2013
NV1350	Implementation of I2C Master Bus Controller on FPGA	2013
NV1351	Novel High Speed Vedic Mathematics Multiplier using Compressors	2013
NV1352	VLSI Implementation of a HighSpeedSinglePrecisionFloatingPointUnit Using Verilog	2013
NV1353	VLSI implementation of Fast Addition using Quaternary Signed Digit Number System	2013
NV1354	Design of High Performance 64bit MAC Unit	2013
NV1355	FPGA Architecture for OFDM Software Defined Radio with an Optimized Direct Digital Frequency Synthesizer	2013
NV1356	Implementation of UART with BIST Technique in FPGA	2013
NV1357	A High Speed Binary Floating Point Multiplier Using Dadda Algorithm	2013
NV1258	Soft-Error-Resilient FPGAs Using Built-In 2-D Hamming Product Code	2012(T)
NV1259	High-Speed Low-Power Viterbi Decoder Design for TCM Decoders	2012(T)
NV1260	Product Code Schemes for Error Correction in MLC NAND Flash Memories	2012(T)
NV1261	Low-Power and Area-Efficient Carry Select Adder	2012(T)

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NV1262	Low-Cost Binary128 Floating-Point FMA Unit Design with SIMD Support	2012(T)
NV1263	Design and Implementation of 64-Bit Execute Stage for VLIW Processor Architecture on FPGA	2012
NV1264	Design and FPGA-based Implementation of a High Performance32-bit DSP Processor	2012

VLSI BACKEND: LOW POWER VLSI PROJECTS

VLSI: M.Tech/M.E IEEE Project List – 2016

CODE	M.Tech VLSI IEEE PROJECTS	YEAR
NL1601	Optimized Active Single-Miller Capacitor Compensation With Inner Half-Feed forward Stage for Very High-Load Three-Stage OTAs	2016(T)
NL1602	Compensation Method for Multi Stage Opamps with High Capacitive Load Using Negative Capacitance	2016(T)
NL1603	Variable-Mirror Amplifier: A New Family of Process-Independent Class-AB Single-Stage OTAs for Low-Power SC Circuits	2016(T)
NL1604	A Low Noise Output Capacitor-less Low Dropout Regulator with a Switched-RC Band gap Reference	2016(T)
NL1605	Integer-N Phase Locked Loop for Bluetooth Receiver in CMOS 130 nm Technology	2016(T)
NL1606	Ultra-low-power one-pin crystal oscillator with self-charged technique	2016(T)
NL1607	High-Performance Low-Cost Dual 15 GHz/30 GHz CMOS LC Voltage-Controlled Oscillator	2016(T)
NL1608	A Power-Efficient Reconfigurable Output-Capacitor-Less Low-Drop-Out Regulator for Low-Power Analog Sensing Front-End	2016(T)
NL1609	Analysis of 8 Bit RCA Adder at Different Nanometer Regime	2016
NL1610	A Novel Power Efficient N-MOS Based 1-Bit Full Adder	2016

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NL1611	Methods of Slew Rate Verification of Operational Amplifier Macro Model	2016
NL1612	A Novel Power Efficient Pulse Triggered Flip Flop with Minimum Transistors	2016
NL1613	Design of Low-Power High-Gain Operational Amplifier for Bio-Medical Applications	2016
NL1614	Low-Complexity Multiternary Digit Multiplier Design in CNTFET Technology	2016(T)
NV1615	A Modified SRAM Based Low Power Memory Design	2016
NV1616	Low Power High Speed D Flip Flop Design using Improved SVL Technique	2016

VLSI: M.Tech/M.E IEEE Project List – 2015

CODE	M.Tech VLSI IEEE PROJECTS	YEAR
NL1501	Low-Power Clock Distribution Using a Current-Pulsed Clocked Flip-Flop	2015(T)
NL1502	Design Methodology of Sub threshold Three-Stage CMOSOT As Suitable for Ultralow-Power Low-Area and High Driving Capability	2015(T)
NL1503	Low–Power and Area-Efficient Shift Register Using Pulsed Latches	2015(T)
NL1504	A Fully-Integrated Low-Dropout Regulator With Full-Spectrum Power Supply Rejection	2015(T)
NL1505	40-Gbs0.7-V21MUXand12DEMUXwithTransformer-Coupled Technique for SerDes Interface	2015(T)
NL1506	Low Power Conditional Pulse Control with Transmission Gate Flip-Flop	2015
NL1507	An Efficient Design Technique for Low Power Dynamic Feed through Logic With Enhanced Performance for wide fan-in gates	2015
NL1508	Performance Analysis of CNTFET Based DigitalLogicCircuits	2015

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NL1509	A 90nm Low Power OTA Using Adaptive Bias	2015
NL1510	Implementing Low-Power Dynamic Adders in MTCMOS Technology	2015
NL1511	Design of high speed ternary full adder and three input XOR circuits using CNTFETs	2015
NL1512	An 8GHz First-Order Frequency Synthesizer for Low-Power On-Chip Clock Generation	2015
NL1513	Free class AB–AB Miller opamp with high current enhancement	2015
NL1514	Ultralow-Energy Variation-Aware Design: Adder Architecture Study	Cadence-2015
NL1515	Designing Tunable Sub threshold Logic Circuits Using Adaptive Feedback equalization	Cadence-2015
NL1516	Design of a Low Power 4x4 Multiplier Based on Five Transistor (5-T) Half Adder, Eight Transistor (8-T) Full Adder & Two Transistor (2-T) AND Gate	2015(T)
NL1517	Dynamic Threshold Source Coupled Logic with Push pull topology for Ultra Low Power Applications	2015
NL1518	Low Voltage Full Swing VCO With Symmetrical Even Phase Outputs Based On Single Ended Delay Cells	2015(T)
NL1519	Recursive Approach to the Design of a Parallel Self-Timed Adder	2015(T)
NL1420	Comparative Performance Analysis of XORXNOR Function Based High-Speed CMOS Full Adder Circuits	2014
NL1421	Analysis and Design of a Low-Voltage Low-Power Double-Tail Comparator	2014(T)
NL1422	A Fault-Tolerant Technique using Quadded Logic and Quadded Transistors	2014(T)

***NOTE*: PLEASE CONTACTUS IF ANY ONE IS INTERESTED TO SELECT CADENCE PROJECTS**